Abstract of the Disclosure

In a CMOS circuit formed on a substrate 101, a subordinate gate wiring line (a first wiring line) 102a and main gate wiring line (a second wiring line) 107a are provided in an n-channel TFT. The LDD regions 113 overlaps the first wiring line 102a and does not overlap the second wiring line 107a. Thus, when a gate voltage is applied to the first wiring line, the GOLD structure is formed, while no applying forms the LLD structure. In this way, the GOLD structure and the LLD structure can be used appropriately in accordance with the respective specifications required for the circuits.